

DETAILED ACTION

1. Referring to the text of the previous office action and phone conversations with Attorney Sarah Knight, and in view of the late date at which the translation of the Fukuzumi reference has become available, examiner herewith vacates the previous office action and replaces said office action with the following office action. Examiner regrets the delay in the availability of the translation.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. ***Claims 1, 2, 4-7 and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud et al (US 2002/0015322 A1) in view of Lee et al (US 2001/0005604 A1) and Noble et al (US 2002/0024083 A1).

Cloud et al teach a semiconductor device (see Abstract), comprising:

a capacitor having a bottom electrode (channel of MOSFET 210) ([0030]), a dielectric layer 213 formed on the bottom electrode, and an upper electrode (gate electrode 212 of MOSFET 210) formed on the dielectric layer, the capacitor being formed on a semiconductor substrate 211([0029]) (see Figure 2);

a first insulating layer 232 formed on the semiconductor substrate covering the capacitor;

while Cloud et al do not specifically disclose the limitation of lines 6-11 of claim 1 but instead omit details on the bitline connections altogether, it would have been obvious to include said limitation in view of Lee et al, who, in a patent application drawn to a DRAM device (see title, abstract and "Background of the Invention"), hence art analogous to Cloud et al, teach:

a plurality of contact plugs 122, 128 formed in a plurality of via holes of the first insulating layer 120, each electrically connected to either the bottom electrode (channel of semiconductor substrate 110 (semiconductive because otherwise the gate action of 114 would not be operative in the transistor) or the upper electrode (gate electrode 114), namely: electrically connected to the bottom electrode (through the source/drain regions 116 and 118) (see Figure 8; also see Figures 1 and 9-10);

a first metal wiring 124 (bitline wiring) formed on the first insulating layer 120 and connected to the bottom electrode through one of the first contact plugs (122);

a second insulating layer (either 126 or 126/136) formed on the first insulating layer.

As shown by Lee et al, the inclusion of the limitation is nothing more than the application of standard, i.e., conventional DRAM device design employing a multi-layer metal interconnection structure (see also Figure 1 in their description of the Prior Art at the time of their filing, which also exhibits the same DRAM bitline design). The limitation is especially obvious in light of the conventional multi-layer construction of DRAM

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devices (see [00006]) in Lee et al) wherein examiner takes official notice that for reason of separate operating function different metal connections are separated by interlayer dielectric.

Furthermore, Cloud et al teach:

a second contact plug 230 in insulating layer 232 ([0030]) and connected to the upper electrode 212;

an anti-fuse (capacitor dielectric 222) ([0030]) [Examiner note: anti-fuse materially is nothing more than a thin dielectric layer, “anti-fuse” distinguishing only intended use] formed on the second contact plug in a second via hole, i.e., via hole in a “subsequent layer” containing capacitor 220, which would have been obviously insulating within the context of aforementioned multi-layered DRAM design; said anti-fuse or capacitor dielectric capable of providing electrical connection of a third contact plug to the second contact plug (see below for an embodiment thereof; however, it is noted that the limitation “for electrical connection to the second contact plug” constitutes only a limitation of intended use); the third contact plug here being the concave central portion of top plate 223, filling the second via hole and formed within the anti-fuse, wherein the third contact plug does not directly contact any underlying insulating layer other than said anti-fuse; and

a second metal wiring (top and side portions of top plate 213) formed on the insulating layer 232 and electrically connected to the third contact plug (through a contiguous connection) and to the anti-fuse (which it abuts and hence exerts capacitive coupling thereon).

Cloud et al do not specifically teach the limitation that the second contact plug is formed in a second insulating layer because as we have seen *Cloud et al* only provide an incomplete teaching of the bitline interconnect. However, following the teaching of *Lee et al* as referred to above, it would have been obvious to locate the capacitor well above and separated by interlayer dielectric from the bit lines, motivation being provided by said separation of functionally independent metal parts: this is what *Lee et al* disclose: capacitor 130/132/134 connected to contact plug (upper portion of 128) in a second insulating layer 126 on a first insulating layer 120. The limitation would have been obvious as nothing more than the application of standard, i.e., conventional DRAM device design employing a multi-layer metal interconnection structure (see also Figure 1 in their description of the Prior Art at the time of their filing, which also exhibits the same DRAM bitline design). The limitation is especially obvious in light of the conventional multi-layer construction of DRAM devices (see [00006]] in *Lee et al*) wherein examiner takes official notice that for reason of separate operating function different metal connections are separated by interlayer dielectric. Incorporation of the teaching by *Lee et al* in the semiconductor device by *Cloud et al* requires nothing more than combining prior art elements according to known methods to yield predictable results: the additional teaching by *Lee et al* only ensures placing bitline metal on a lower interlayer dielectric than the capacitor. In the invention by *Cloud et al* the capacitor is placed on the gate of the transistor and hence both source and drain interconnects could connect at a comparable, and lower interlayer dielectric level than the level of the capacitor, as

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confirmed by Noble et al (US 2002/0024083 A1) (see source line 217A and bit line 219A in vertical relation to the capacitor 220; Figure 2 and [0047]-[0049]).

On claim 2: first and second metal wiring are perpendicular to each other (word line WL and bitline BL; see Fig. 1; word line is tied to second wiring (top plate 223) (Figure 2 and [0011]) (see also Noble et al; Figure 2 and [0047]-[0049]).

On claim 5: in the combined invention, wherein the interlayer dielectrics are taken from Lee et al, the upper surface of the third contact plug and the upper surface of the second insulating layer are at least substantially in the same horizontal plane; namely: the upper plane boundary, on the right-hand side, of 126/136 (see Figures 8-10). Applicant does not disclose the specific equality of heights, implicitly an extremely narrow range limitation, to be critical to the invention. Its incorporation in a dependent claim only is evidence to the contrary. Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

On claims 4 and 7: in the combined invention, the anti-fuse 222 is formed between the second contact plug 230 and the third contact plug (inner, central portion of 223) and between the second insulating layer (which, following Lee et al takes up the uppermost portion of 232) and the third contact plug (inner central portion of 223 between the vertical parts of 222).

On claims 6 and 10: the range limitation on relative width of the third contact plug to that of the second contact plug recited by claim 6 has not been disclosed as critical to applicant's invention. On the contrary, said range limitation evidently is not critical to the invention, because claim 1 defines an acceptable invention by applicant and does not contain the limitation of said range. Applicant is reminded that Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

4. **Claims 3, 8 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud et al (US 2002/0015322 A1) in view of Lee et al (US 2001/0005604 A1), Noble et al (US 2002/0024083 A1) and Yamauchi et al (US 2001/0045667 A1).

The device of claim 1 would necessarily have to be formed in order to function. With the potential exception of the steps of patterning and planarizing as recited, claims 3 and 8 fail to further limit the device of claim 1 other simply form their components. However, both the methods of forming a plurality of via holes by patterning an insulation layer and forming a conductive layer and contact plug by planarizing metal layers have long been known and conventional in the art of making interconnects including vias, as shown, for instance, by Yamauchi et al, who teach (a) (see Figure 2(d)) the making of a plurality of via holes in a desired configuration by patterning ([0051]), and (b) (see Figure 1(c) and [0065]) making conductive material in plugs through planarizing metal layers with the

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insulating layer (hence claim 9 is met as well) in which said conductive material in plugs are intended to be located. The particular teaching by Yamauchi et al as defined above is amply sufficient to complete the claimed method when applied to the steps of forming a plurality of via holes and second via hole as well as forming an anti-fuse on the second contact plug in the second via hole and a third contact plug within the anti-fuse by planarizing the first and second metal layers with the second insulating layer, because, given the structure of the invention, nothing more than the application of patterning the plurality of via holes and the step of planarizing taught by Yamauchi et al is needed to arrive at the claimed method. Therefore, nothing more is involved than “combining prior art elements according to known methods to yield predictable results”, On account of which the claim would have been obvious to one of ordinary skill in the art.

Response to Arguments

5. Applicant's arguments, see Remarks filed 9/24/08, with respect to the rejection over Fukuzumi have been fully considered and are persuasive, because the translation as prepared by the Translations Branch of the U.S. Patent & Trademark Office shows that, although word lines are disclosed to connect to the upper electrodes identified in the rejection with the gate electrodes, they do not necessarily connect to said upper electrodes through any second contact plug in the second insulating layer formed on the first insulating layer, being connected to the upper electrode (gate electrode) through another one of said first contact plugs. In this regard it is noted that layer 14 is not

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necessarily conductive, and is, e.g., made of insulator material SiN. Layer 11 is not necessarily “optional”, but instead is “selectively” applied.

Accordingly, the rejections over Fukuzumi of claims 1-10 under 35 USC 103(a) as being unpatentable over Fukuzumi in view of Cooney III et al have been withdrawn. Based upon further consideration and search a ground of rejection over Cloud et al (US 2002/0015322 A1) in view of Lee et al (US 2001/0005604 A1) and Noble et al (US 2002/0024083 A1) is herewith presented for claims 1, 2, 5-7 and 10, while claims 3, 8 and 9 are rejected over these three references supplemented by Yamauchi et al (US 2001/0045667 A1). Examiner appreciates Attorney's expression of concern over the rejections of the method claims, which he believes are addressed by the additional references to Yamauchi et al.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 7:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Johannes P Mondt/
Primary Examiner, Art Unit 3663